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METHOD AND APPARATUS OF COUPLING CONDUCTORS IN MAGNETIC MEMORY

BACKGROUND

[0001] Memory devices are ubiquitous in numerous fields involving computers and electronics. In some cases, memory has been implemented with storage elements capable of storing electrical charge. In other cases, memory has been implemented with storage elements capable storing magnetic orientation. Solid-state magnetic memory arrays may comprise individual storage elements constructed utilizing semiconductor processing techniques.

[0002] The individual magnetic elements of the magnetic memory array may comprise materials with varying magnetic properties separated by an insulating layer. The magnetizations of the separated materials may be oriented in the same direction (termed "parallel"), or their orientation may be opposite directions (termed "anti-parallel"). The electrical resistance of the magnetic elements may vary depending on the parallel or anti-parallel orientation of the magnetizations. In this manner, digital information may be stored and retrieved by associating digital values (e.g., 1s and 0s) to the electrical resistance associated with the parallel and anti-parallel states.

[0003] The orientation (i.e., parallel or anti-parallel), and consequently the digital value, of a memory element may be configured by inducing a magnetic field in the memory element. Conductors that may be proximate to the memory element may conduct current, and this current may consequently induce a magnetic field in the proximate memory element. The induced magnetic field may then change the orientation of the memory element.

[0004] Because memory is often employed in consumer electronics, memory that is high speed, low cost, and low power is desirable. The power consumption, speed, and cost of the memory chip are directly related to the total chip area (i.e., the area of the array of memory elements and accompanying circuitry), and larger chips may be more costly to manufacture. As a result, low cost memory may be built by densely packing memory elements within a memory array. However, the conductors used in configuring the memory elements may undesirably limit the density of the memory elements and add to the size of the chip.

[0005] Therefore, it may be difficult to design memory that is fast, cheap, and that consumes low power because the techniques for increasing speed and decreasing power often lead to cost increases and vice versa.

BRIEF SUMMARY

[0006] Methods and apparatuses are disclosed for coupling conductors in magnetic memory. In some embodiments, the memory element may comprise: a first magnetic memory element, a first group of conductors magnetically coupled to the first magnetic memory element, a second magnetic memory element, a second group of conductors magnetically coupled to the second magnetic memory element, where the second magnetic memory element is substantially vertical to the first, and the first and second group of conductors may have at least one conductor in common.

BRIEF DESCRIPTION OF THE DRAWINGS

[0007] For a detailed description of the various embodiments of the invention, reference will now be made to the accompanying drawings in which:

[0008] Figure 1 illustrates an exemplary computer system in accordance with various embodiments of the invention;

[0009] Figure 2A illustrates a substrate in wafer form in accordance with various embodiments of the invention;

[0010] Figure 2B illustrates a simplified cross-section of an integrated circuit containing magnetic memory in accordance with various embodiments of the invention;

[0011] Figure 3 illustrates an exemplary implementation of a magnetic memory element in accordance with embodiments of the invention;

[0012] Figure 4A illustrates an exemplary relationship between the axes of magnetic orientation of an exemplary memory element in accordance with embodiments of the invention;

[0013] Figure 4B illustrates an exemplary relationship between the axes of magnetic orientation of an exemplary memory element, where the hard axis is altered in accordance with embodiments of the invention;

[0014] Figure 5 illustrates an exemplary implementation of a magnetic memory element including read and write conductors in accordance with embodiments of the invention; and

[0015] Figure 6 illustrates an exemplary embodiment of magnetic memory elements arranged vertically in accordance with embodiments of the invention.

NOTATION AND NOMENCLATURE

[0016] Certain terms are used throughout the following description and claims to refer to particular system components. As one skilled in the art will appreciate, companies may refer to a component by different names. This document does not intend to distinguish between components that differ in name but not function. In the following discussion and in the claims, the terms "including" and "comprising" are used in an open-ended fashion, and thus should be interpreted to mean "including, but not limited to..." Also, the term "couple" or "couples" is intended to mean either an indirect or direct electrical or mechanical connection. Thus, if a first device couples to a second device, that connection may be through a direct connection, or through an indirect connection via other devices and connections. The phrase "magnetically coupled" is intended to refer to the situation in which a magnetic field emanating from a first material is induced in second material. For example, a conductor carrying a current may emanate a magnetic field that may be coupled into a magnetic material. Also, the term "easy axis" current refers to current that produces a magnetic field along the easy axis of a magnetic memory element. Likewise, the term "hard axis" current refers to a current that produces a magnetic field along the hard axis of a magnetic memory element.

DETAILED DESCRIPTION

[0017] The drawings and following discussion are directed to various embodiments of the invention. Although one or more of these embodiments may be preferred, the embodiments disclosed should not be interpreted, or otherwise used, as limiting the scope of the disclosure. In addition, one skilled in the art will understand that the following description has broad application, and the discussion of any embodiment is meant only to be exemplary of that embodiment, and not intended to intimate that the scope of the disclosure, is limited to that embodiment.

[0018] The memory disclosed herein, and the methods for reducing memory power consumption, may be used in a computer system. Figure 1 illustrates an exemplary computer system 100. The computer system of Figure 1 includes a CPU 102 that may be electrically coupled to a bridge logic device 106 via a CPU bus. The bridge logic device 106 is sometimes referred to as a "North bridge." The North bridge 106 may electrically couple to a main memory array 104 by a memory bus, and may further electrically couple to a graphics controller 108 via an advanced graphics processor (AGP) bus. The North bridge 106 may couple CPU 102, memory 104, and graphics controller 108 to the other peripheral devices in the system through, for example, a primary expansion bus (BUS A) such as a PCI bus or an EISA bus. Various components that operate using the bus protocol of BUS A may reside on this bus, such as an audio device 114, and a network interface card (NIC) 118. These components may be integrated onto the motherboard, or they may be plugged into expansion slots 110 coupled to BUS A.

[0019] The main memory array 104 may be manufactured using semiconductor processing techniques. Figure 2A illustrates a semiconductor substrate 210 in wafer form. Substrate 210 may comprise silicon, germanium, gallium arsenide, or other elements that have semiconducting properties. Circuitry and memory elements may be integrated on side 210A of the substrate while opposite side 210B may remain substantially void. Figure 2B illustrates a simplified cross section of substrate 210 including circuitry 212 and memory elements 214 integrated on the substrate 210. Circuitry 212 may comprise complementary

metal oxide semiconductor (CMOS) type transistors. Other technologies (i.e., bipolar, JFET) may alternatively be used. Circuitry 212 may implement circuitry for writing and reading digital information to and from magnetic memory 214. Because different material and techniques may be used, circuitry 212 and memory 214 may be manufactured separately. For example in Figure 2B, the transistors in circuitry 212 may be integrated on the integrated circuit prior to integrating the memory elements of memory 214.

[0020] Magnetic memory 214 may comprise memory elements, where information may be stored in the memory elements by altering their magnetic state. Figure 3 illustrates an implementation of a memory element 215 and associated conductors 216 and 217 which may be used to write the memory element. Memory element 215 may comprise a reference layer 215A, which in some embodiments has a magnetization with fixed orientation (as illustrated by the single sided dashed arrow). In these embodiments, layer 215A may be referred to as the "pinned" layer because of its fixed orientation. Memory element 215 may also include another layer 215B, integrated on top of layer 215A, with an insulating layer 215C disposed between layers 215A and 215B. In this manner, layers 215A and 215B may form a sandwich-like structure around layer 215C. In some embodiments, layer 215B may have a magnetization with variable orientation (as illustrated by the double sided dashed arrow). By exposing the magnetic layer 215 to a magnetic field in a particular direction, the orientation of the magnetization in the magnetic layer 215B may be changed. Thus, layer 215B may be referred to as the "data" layer because it may store the orientation of the memory element 215 with respect to layer 215A, which may have fixed orientation.

[0021] The magnetic layers 215A and 215B of memory element 215 may be preconfigured to favor a particular axis for the orientation of magnetization. The favored orientation of magnetization is sometimes referred to as the "easy axis." For example, the easy axis of magnetic layer 215B is labeled E_A in Figure 3. Similarly the non-favored orientation of magnetization is sometimes referred to as the "hard axis." The hard axis of layer 215B, labeled H_A in Figure 3, may be orthogonal to the easy axis. The memory element 215 may be configured such

that the magnetic fields required to change the magnetic orientation of a magnetic layer may be less along the easy axis than along the hard axis.

[0022] Figure 4A illustrates an exemplary relationship between the absolute value of magnetic fields along the easy axis (B_E) and the absolute value of magnetic fields along the hard axis (B_H) as they relate to changing of the magnetic orientation of the magnetic layer. The curve illustrated in Figure 4A may represent the magnetic threshold at which a magnetization orientation of a magnetic layer (such as layer 215B in Figure 3) may switch. A magnetic layer may be subject to a net magnetic field comprising a component in the easy axis B_E direction, and a component in the hard axis direction B_H. When the magnetic layer experiences a net magnetic field that is above the magnetization threshold (illustrated in Figure 4A), the magnetic orientation of the magnetic layer may be changed. Yet, beneath the magnetization threshold, the net magnetic field applied to the magnetic layer may not be enough to cause the orientation of the magnetic layer to change.

[0023] For example, the magnetization threshold illustrated in Figure 4A may correspond to the magnetization characteristics of layer 215B illustrated in Figure 3. Current in conductor 216 may induce a magnetic field aligned with the hard axis (indicated as B_{H1} in Figure 4A), and current in conductor 217 may induce a magnetic field aligned with the easy axis (indicated as B_{E1}). The dashed lines in Figure 4A indicate that the magnetic field components B_{E1} and B_{H1} together may result in a net magnetic field at point A. Since the net magnetic field at point A is beneath the magnetization threshold, the net magnetic field may not be sufficient to cause the magnetic orientation of the magnetic layer to change. However, if the hard axis component is increased to B_{H2} (as indicated by the dashed line) while the easy axis magnetic field is held constant at B_{E1}, then the net magnetic field at point B may be sufficient to cause the orientation of the magnetic layer to change. The relationship depicted in Figure 4A is merely illustrative and other viable relationships may exist. For example, magnetic layers may be fabricated with an inherent alteration in the magnetization threshold in either the hard or easy axes, as illustrated in Figure 4B.

[0024] Referring to Figure 4B, the magnetization threshold may be altered in the direction of the hard axis B_H. Altering the hard axis may be accomplished in various ways, such as by rotating the magnetic memory element 215 with respect to the conductors 216 and 217. In these embodiments, inducing a magnetic field along the easy axis alone may be enough to cause the orientation of the magnetic layer to change. For example, as indicated in Figure 4B, the easy axis field B_{E2} at point C alone may be sufficient to overcome the magnetic threshold and cause the magnetic orientation of the magnetic layer to change.

[0025] Referring again to Figure 3, the orientation of the magnetization of layer 215B may be adjusted to be parallel to the magnetization of layer 215A (i.e., arrows in the same direction), or anti-parallel to the magnetization of layer 215A (i.e., arrows in opposite directions). By varying the relative magnetic orientations (parallel or anti-parallel) of layers 215A and 215B, the electrical resistance of layer 215C may be varied. Digital values may be stored by associating the various electrical resistances of layer 215C with the digital values. Accordingly, the memory element 215 is sometimes referred to as a magneto-resistive tunnel junction (MTJ). For example, a voltage potential may be established across memory element 215, which may cause current carriers to "tunnel" through layer 215C. The electrical resistance to the flow of current may be characterized and associated with a digital value—e.g., 1 MΩ may be measured and associated with a digital 0, and 1.1 MΩ may be measured and associated with a digital 1.

[0026] In order to store data values to memory element 215, write lines 216 and 217 may be employed. The separation distance illustrated in Figure 3 between the write lines 216 and 217 and the memory element 215 is exaggerated for clarity, and in accordance with embodiments of the invention the actual separation distance may be on the order of a few hundred angstroms or less. Alternative embodiments may comprise lines 216 and 217 in direct physical contact with memory element 215 with no dielectric separating the memory element 215 from either line 216 or 217. Circuitry (not illustrated in Figure 3), may be electrically coupled to write lines 216 and 217 to provide electrical currents I_1 and I_2. Current I_1 in write line 216 may generate a magnetic field B_1, and likewise current I_2 in write line 217 may generate a magnetic field B_2. Magnetic fields B_1

and B_2 may then collectively contribute to the magnetic field induced in memory element 215, where the magnetic fields B_1 and B_2 may be adjusted by adjusting the strength and direction of currents I_1 and I_2. For example, reversing the direction of the currents I_1 and I_2 will reverse the orientation of the magnetic fields B_1 and B_2. Accordingly, the orientation of the magnetizations in layers 215A and 215B may be adjusted to be parallel or anti-parallel. As was mentioned above, the magnetic memory element 215 may be subject to adjusting the inherent magnetization, which may alter the memory element's switching characteristics, as is illustrated in Figure 4B.

[0027] Figure 5 illustrates the memory element 215 of Figure 3 in greater detail and including read lines 218 and 219. In order to read data from a memory element, read lines 218 and 219 may be electrically coupled to the memory element as illustrated in Figure 5. An inter-layer dielectric (ILD) 220 may electrically isolate write line 216 from read line 218. Likewise, ILD 221 may electrically isolate write line 217 from read line 219. While ILDs 220 and 221 are illustrated separating read and write lines in Figure 3B, subsequent figures may not show an ILD to separate read and write lines for the sake of clarity. It should be understood that an ILD may be included between any read and write conductor pair for electrical isolation. Additionally, although read line 218 and write line 216 are illustrated running in the same direction, this embodiment is not required; and read line 218 and write line 216 may be oriented in any direction with respect to each other. Similarly, read line 219 and write line 217 may also be oriented in any direction with respect to each other. Circuitry (not illustrated in Figure 5) may be electrically coupled to read lines 218 and 219 in order to facilitate reading of memory element 215.

[0028] In accordance with embodiments of the invention, high density memory arrays may be integrated on the substrate adjacent to each other. Figure 6 illustrates magnetic memory elements 222 and 223 that are substantially vertical to each other. Although Figure 6 illustrates memory element 222 directly below memory element 223, there may be a lateral offset between the memory elements 222 and 223. Memory element 222 may be electrically coupled to read conductors 225 and 226. Read conductors 225 and 226 may be used to

determine the digital state of memory element 222. Similarly, read conductors 227 and 228 may be coupled to magnetic memory element 223, and read conductors 227 and 228 may be used to determine the digital state of memory element 223.

[0029] Memory element 222 may be magnetically coupled to write conductors 229 and 230. Write conductors 229 and 230 may be used to adjust the magnetic orientation of memory element 222. Likewise, write conductors 230 and 231 may be magnetically coupled to memory element 223, and write conductors 230 and 231 may be used to adjust the magnetic orientation of memory element 223. By integrating the memory elements 222 and 223 on top of each other, common write conductors may be shared between the memory elements 222 and 223. For example, write conductor 230 may magnetically couple to both memory element 222 and memory element 223. In this manner, one or more conductors may be eliminated so that fewer processing steps may be required to manufacture the memory devices. In addition, inducing currents in the various conductors associated with magnetic memory elements consumes power, and therefore reducing the number of the conductors used to perform memory operations consequently may also reduce the amount of power consumed.

[0030] The easy axes of memory elements 222 and 223 may be configured in the Y direction and the hard axes may be configured in the X direction, where the X, Y, and Z directions are indicated in Figure 6. In this configuration, currents that flow in write conductors 229 and 231 may contribute to the easy axis field, and currents that flow in the common write conductor 230 may contribute to the hard axis field. Thus, in changing the magnetic orientation of memory elements 222 and 223, a hard axis current may flow in conductor 230. The hard axis current alone will not be sufficient to change the magnetic orientation of memory elements 222 or memory element 223. This situation was depicted with regard to point A in Figure 4A. In order to change the orientation of the memory elements, an easy axis current may be required in the memory element's easy axis write conductor. For example, with a hard axis current flowing in conductor 230, the magnetic orientation of the magnetization of memory element 222 may be

changed by inducing an easy axis current in conductor 229. Also, with a hard axis current flowing in conductor 230, the orientation of the magnetization of memory element 223 may be changed by inducing an easy axis current in conductor 231. Therefore, memory elements 222 and 223 may independently have their magnetic orientations, and consequently their digital states, changed. Memory elements 222 and 223 may be written simultaneously by applying currents to conductors 230, 229, and 231. Therefore, two memory elements may be written using three currents, and the amount of energy utilized may therefore be reduced.

[0031] Alternatively, if the easy axes of memory elements 222 and 223 run in the X direction, then current in common write conductor 230 produces an easy axis field. Memory elements 222 and 223 may be written to simultaneously, for example, by inducing a current in the common write conductor 230 as well as conductors 229 and 231.

[0032] In addition, the easy or hard axes may be altered such that memory elements may be written to by applying only easy or hard axis current. For example, an alteration may be introduced in the memory elements such that the switching threshold illustrated in Figure 4B applies. In these embodiments, the orientation of the memory elements may be changed by applying only easy axis fields, e.g., point A in Figure 4B. Thus, referring back to Figure 6, if the memory element 222 includes an altered magnetization threshold characteristic, then a current in write conductor 229 alone may allow the orientation of memory element 222 to be changed. Likewise, if memory element 223 includes an altered magnetization characteristic, current in write conductor 231 alone may be sufficient to change the orientation of memory element 223.

[0033] The common write conductor 230 may be used to selectively write data to memory elements 222 and 223. For example, the structure illustrated in Figure 6 may be implemented in an array of memory elements where many memory elements are coupled to write conductor 230. Thus, if conductor 230 represents easy axis current, then all of the memory elements in the array that are magnetically coupled to write conductor 230 may be altered simultaneously by inducing a sufficient amount of current in common write conductor 230. For example, all the memory elements that are magnetically coupled to write

conductor 230 may be written to 1. Subsequently, desired memory elements may be written to the opposite digital state by reducing the current in the common write conductor 230 (easy axis current) while inducing the appropriate current in the write conductor 229 and/or 231 (hard axis current). In this manner, memory element 222 and/or 223 may be selectively written to a desired digital state using three conductors, which may result in overall power savings.

[0034] The non-destructive read techniques disclosed in U.S. Patent Application No. 10/465,714, entitled "Retrieving Data Stored in a Magnetic Integrated Memory" (Atty. Docket No. 200205501-1), which is incorporated herein by reference, may be implemented in the various embodiments disclosed herein. For example, referring to Figure 6, read circuitry (not illustrated in Figure 6) may monitor the resistance of memory element 222 via read conductors 225 and 226. Concurrently, current may flow in the common write conductor 230, which in this example, may induce a field along the hard axis of memory element 222. The magnetic field induced along the hard axis will not be sufficient to alter the magnetic orientation of the memory element 222. However, hard axis magnetic fields may be sufficient to temporarily perturb the resistance of memory elements as the magnetic field is turned on and off. By monitoring the rate of change of the resistance of memory element 222 as the current is switched, the orientation of the magnetization of memory element 222 may be determined. In addition, since conductor 230 may magnetically couple to both memory element 222 and memory element 223, conductor 230 may be used to determine the orientation of memory element 222 and memory element 223 simultaneously. Therefore, memory read time may be reduced as multiple memory elements may be read simultaneously.

[0035] The above discussion is meant to be illustrative of the principles and various embodiments of the present invention. Numerous variations and modifications will become apparent to those skilled in the art once the above disclosure is fully appreciated. For example, although magneto-resistive memory elements were disclosed in conjunction with some of the embodiments of the invention, other memory devices with variable resistances may be implemented without departing from the scope of this disclosure.

[0036] In addition, although Figure 6 shows two memory elements substantially vertical to each other, additional stacking may be implemented. For example, multiple memory elements may be stacked substantially vertical with respect to each other, where magnetic conductors are sandwiched between the magnetic memory elements. In this manner, the sandwiched conductors may be used to adjust the magnetic state of the stacked magnetic memory elements. Furthermore, the configuration of the easy and hard axes may be configured in any direction, and the roles of the easy and hard axes as described herein, may be reversed. Additionally, memory elements that are vertically adjacent to each other may be written in opposite digital states using the common conductor. For example, the bottom memory element may be written low and the top memory element may be written high. In this manner, differential sensing techniques may be performed on both the top and bottom memory elements such that accuracy of the read operations may be increased. It is intended that the following claims be interpreted to embrace all such variations and modifications.